# High Performance Low Current CDMA Receiver Front End using 0.18 um SiGe BiCMOS

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*Abstract* — **Silicon Germanium Bipolar CMOS (SiGe BiCMOS) process technology is gaining popularity for RF circuits in wireless applications due to high performance, low cost, high yield and levels of integration with mixed signal and digital CMOS circuits. A tri-band quad mode CDMA RF receiver front end is designed in a 0.18 um SiGe BiCMOS process that enabled LNAs with sub 1dB noise figure and low-noise high-linearity mixers with low current consumption.**

## I. Introduction

The RF performance achievable by silicon based front ends has been considered somewhat inferior compared to GaAs discrete components. Critical performance metrics like low noise figure and high linearity of a radio, as required by IS 95 / CDMA2000 cellular wireless handsets, pose technical challenges to RF IC designers. The performance of the device presented in this paper proves that 0.18um SiGe BiCMOS is the low cost alternative to GaAs process. This device contains low noise amplifiers (LNAs) and mixers in 800MHz (CDMA) / 1900MHz (CDMA-PCS) band and an LNA in 1700 MHz (GPS) band. The die is packaged in a 4X4 RF Land Grid Array (LGA). The receiver front end was designed to provide healthy performance margins on IS 95 / CDMA2000 handsets in AMPS, CDMA and CDMA-PCS modes.

## II. PROCESS TECHNOLOGY

The process technology for this device is the SiGe 0.18um BiCMOS process technology from Jazz Semiconductor Inc [1, 2]. The features of the technology include two types of SiGe NPN transistors (low voltage and high voltage), 3.3 V CMOS, poly resistors, high quality (Q) inductors, and metal to metal (MIM) capacitors. The open base breakdown voltage (BVCEO) is 3.5 V for the low voltage SiGe NPN and 6 V for the high voltage SiGe NPN. The cut-off frequency (ft) is 75 GHz for the low voltage SiGe NPN and 34 GHz for the high voltage SiGe NPN. The Fmax is 130 GHz for the low voltage NPN and 60 GHz for the high voltage NPN. The chip was fabricated with three metal layers. The substrate resistivity is 8 ohm-cm.

## III. TOP LEVEL BLOCK DIAGRAM

The chip includes two LNAs for 1900 MHz and 800MHz bands with external input and output matching. The 800MHz LNA is used for both CDMA and AMPS mode. The 1900 MHz LNA has two gain steps and the 800 MHz LNA has three gain steps. The 1700 MHz GPS LNA has only one gain step.

Two low current double balanced mixers in two bands provide down conversion to the IF frequency which can be varied. CDMA and AMPS modes use the same mixer input. Low current tuned LO limiters are used to switch the mixer cores. LO input to the chip is dual band and does not need external matching.

The block diagram is shown in Fig 1. A detailed description is provided in the following sections.

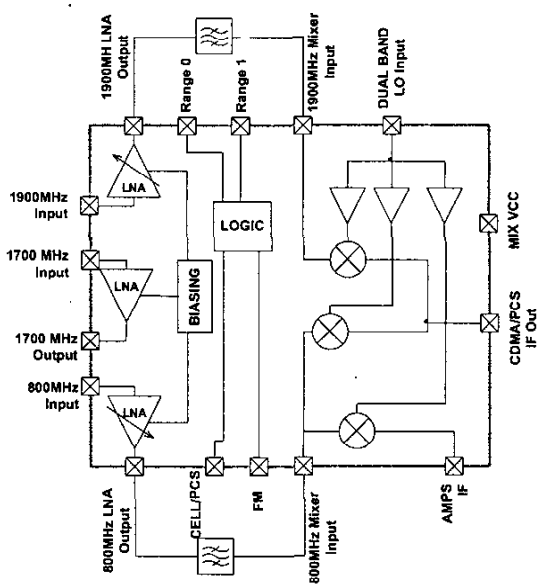


Fig. 1. This figure shows the top level of tri-band quad-mode CDMA receiver front end.



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## V. INDIVIDUAL BLOCK DESCRIPTION

### *A. Low Noise Amplifiers*

Cellular CDMA handsets need to comply with IMD specifications stipulated by TIA/EIA-98-C translate to stringent cascaded input third order inter-modulation product (IIP3). The performance specifications are guaranteed by measurement of intermodulation spurious attenuation at three signal levels with two tones with jammer levels 58 db above the signal in each case. This requires higher IIP3 for higher signal levels. On the other hand, with the increased signal levels, the system gain required is lower and noise figure (NF) allowed is higher. The switched gain LNA with three steps (high-gain, mid-gain, and by-pass mode) is designed to meet the above system requirement. Two control pins are used to switch the gain of LNA.

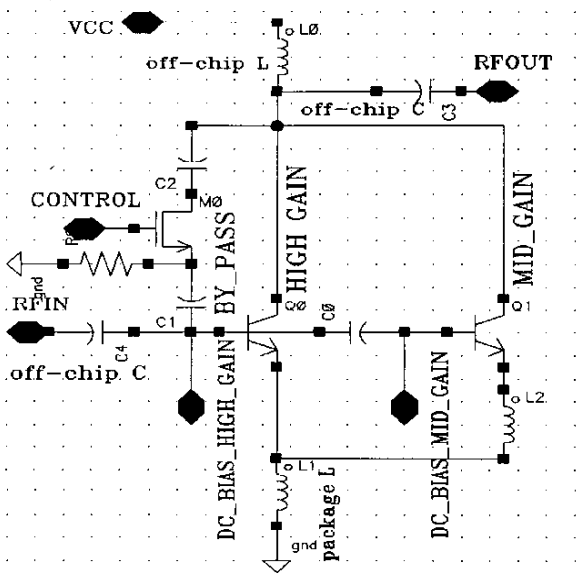


Fig. 2 Simplified schematic of CDMA LNA

Fig. 2 shows a simplified schematic of a switched gain LNA. The high-gain stage is a common emitter NPN with about 2 nH of inductive degeneration from package parasitic. The mid-gain stage is a common emitter NPN with about 8.5 nH of inductive degeneration from both an on chip inductor and package parasitic. The by-pass mode is a NMOS switch. All three branches share one RF input and RF output, therefore, they share the same input and output matching networks. On-chip high quality MIM capacitors are used to separate three branches, so that the three branches can have independent DC bias circuits.

The current used to bias the LNA is generated through a constant voltage (band-gap voltage) and an external resistor. Control logic circuits are used to switch gain modes. When the high-gain stage is on, the mid-gain stage and by-pass stage are off and vice versa.

The emitter width of SiGe NPN transistors for both high-gain and mid-gain is 0.2 um. The emitter lengths of the SiGe NPN were scaled to get an optimum Noise Figure (NF), Gain, IIP3, and input return loss (S11).

One advantage of SiGe NPN over Si NPN is that SiGe NPN has much smaller base resistance than Si NPN does. Small base resistance results in both a lower minimum noise figure (NF_min) and a lower noise resistance (rn). Fig. 3 is a simulated noise circle of high gain mode on a 50 ohm normalized Smith chart. The smallest circle in the Smith chart is the 0.9 dB noise circle, and the largest circle is the 1.2 dB noise circle. As seen in Fig. 3, the DC bias condition and device size of the high gain stage are designed to have the optimum noise point close to 50 ohm point, so that only one DC blocking capacitor is used for input matching.

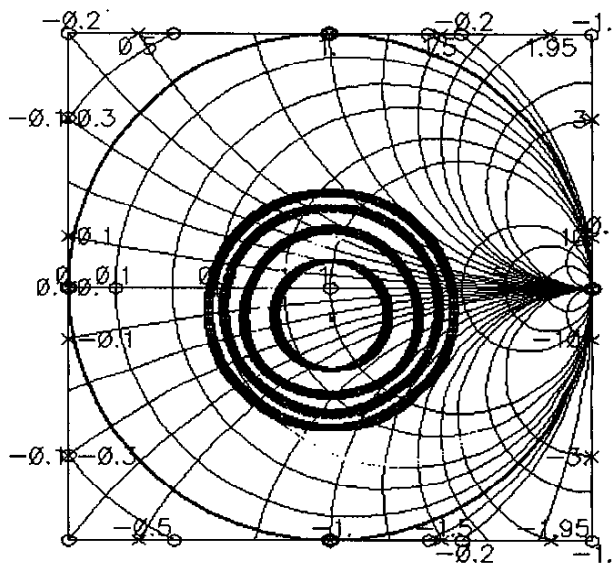

Fig. 3 Simulated noise circles of high-gain mode cell LNA

The PCS LNA has a similar topology to the cellular LNA, but without the mid-gain stage. Three down bonds are used to reduce emitter degeneration at 1.96 GHz PCS frequency. The GPS LNA is similar to PCS LNA without the bypass stage.

### *B. Mixers*

All the mixers are double balanced with inductive degeneration to achieve high linearity as shown in Fig 4. The core transistors are sized for low base resistance without degrading their frequency performance. Lower current consumption helps lowering noise figure. The IF output is differential with external tuning. The LO limiters are differential amplifiers with tuned loads. An LO limiter with a tuned load can attain a high load impedance thus allowing low current consumption for a given LO voltage swing. The LO swing at the switching core of the mixer is important for noise figure considerations. A band gap circuit using an external resistor generates the bias currents for the mixers. The CDMA and PCS mixers share the IF output as shown in Fig. 5.

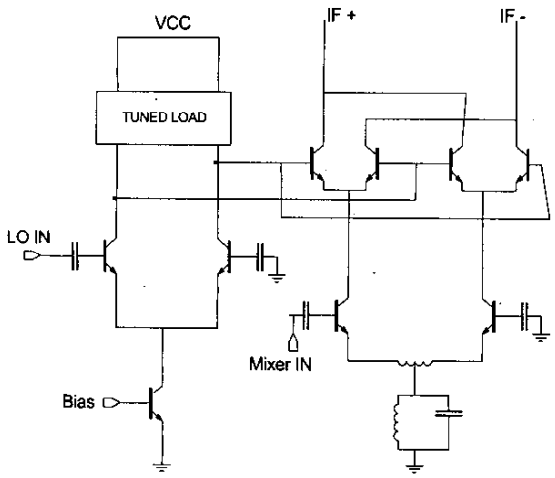


Fig. 4. Double balanced mixer with inductor degeneration. LO limiter is tuned around the LO frequency.

The resonant frequency of the tuned circuit at common emitters of the core transistors of the mixers is adjusted to the RF input frequency of interest. The Q of this circuit is optimized both for high impedance at resonance and minimum process variations of the resonant frequency. This helps in achieving higher differential gain with less current consumption.

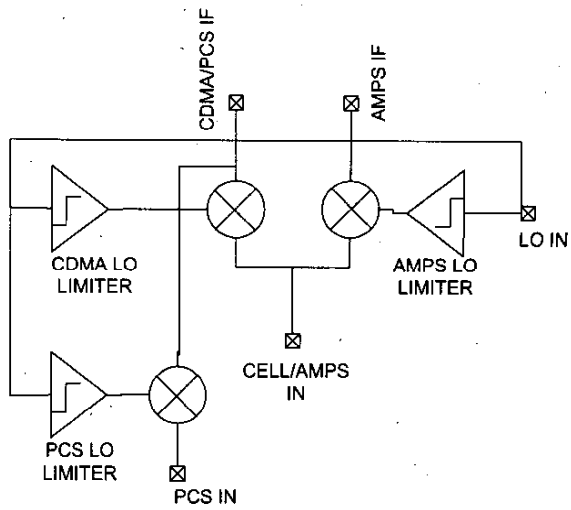


Fig. 5. Mixer scheme used for the SIF and AMPS IF plan shows the separate LO limiters used to enable different mixers

## VI. MEASUREMENT RESULTS

Measurements were carried out on the individual blocks and cascaded performance was calculated based on some assumptions. The results are described in the following three sections.

### A. Low Noise Amplifiers:

Table I. Measured performance of LNAs

| Type | Gain mode | Gain (dB) | NF ( dB) | IIP3 (dBm) | Current (mA) |
|---|---|---|---|---|---|
| Cellular LNA | High gain | 15.4 | 0.95 | 10.5 | 6 |
| | Mid Gain | 4.5 | 3.5 | 17 | 4.5 |
| | Bypass | -6 | 7.3 | 20 | 0 |
| | AMPS | 14.6 | 1 | 3.5 | 3.4 |
| PCS LNA | High gain | 16.5 | 1.1 | 8.5 | 7.6 |
| | Bypass | -3 | 4.3 | 22 | 0 |
| GPS LNA | | 19 | 1 | 7 | 5.5 |

Table I lists the measured performance of three types of LNAs. The DC supply voltage of these measurements is 2.78V. Noise Figure (NF) was measured on HP8970B noise meter. IIP3 was measured at –22 dBm of input power and 1MHz of tone space.

As seen from Table I, in high gain mode, the noise figures of the cellular and PCS LNA are 0.95 dB and 1.1 dB, respectively. This is a 0.7 dB improvement over a

previous CDMA frond end receiver with a similar architecture [3]. At high gain mode, IIP3 of the cellular and PCS LNA are 10.5 dBm and 8.5 dBm respectively. This is about 4- dBm improvement over the previous chip.

*B. Mixers*

Table II lists the measurements on mixers. The input power level for two-tone measurements was –25 dbm and the tone spacing was 1 MHz. The inputs were matched for a –14 db return loss. The output was tuned to 183.6 MHz for CDMA and PCS SIF output and 128.1 MHz for AMPS IF.

Table II. Measured performance of Mixers

| | Gain (db) | NF (db) | IIP3 (dbm) | Current (mA) |
|---|---|---|---|---|
| CELL | 11.4 | 5.5 | 5.4 | 10.5 |
| AMPS | 10.8 | 7.5 | 5.2 | 10.5 |
| PCS | 10.2 | 6.8 | 9.5 | 11.2 |

CELL mixer noise figure is 5.5 db and the current is 10.5 mA. This is an improvement of 2.7 db in noise figure and 7.5 mA in current as compared to the CELL mixer in [3]. In PCS mixer, improvement in noise figure is 1.7 db and current is 6.8 mA. AMPS mixer shows improvement of 0.8 db in noise figure. Table III shows calculated cascaded performance.

Table III. Calculated cascaded performance of the front end.

| Mode | Cascaded[1, 2] NF (dB) | Cascaded IIP3 (dBm) |
|---|---|---|
| CELL CDMA | 1.5 | -7.1 |
| PCS CDMA | 1.7 | -4.2 |
| CELL AMPS | 2.0 | -6.8 |

Note:
1. Cascaded stages include LNA, RF SAW filter, and Mixer.
2. RF SAW filter insertion loss assumed to be 3 dB.

## VII. Conclusion

A low current high performance tri-band quad-mode CDMA front-end receiver device is presented. The measurements of this device prove that low cost SiGe process can replace GaAs process for the future CDMA RF front ends.


## Acknowledgement

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## References


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[3] Keith Rampmeier et al, 2001 *RFIC technical Digest*